Functional overview STM32L476xx

Figure 3. Clock tree to IWDG LSI RC 32 kHz LSCO to RTC and LCD OSC32_OUT LSE OSC /32 OSC32_IN 32.768 kHz LSE LSI HSE MCO / 1→16 to PWR SYSCLK HSI to AHB bus, core, memory and DMA Clock source AHB HCLK FCLK Cortex free running clock control OSC_OUT PRESC HSE OSC 4-48 MHz / 1,2,..512 to Cortex system timer HSE / 8 OSC_IN Clock MSI SYSCLK detector APB1 PCLK1 HSI PRESC to APB1 peripherals / 1,2,4,8,16 x1 or x2 to TIMx 16 MHz x=2..7 LSE HSI SYSCLK to USARTx X=2..5 to LPUART1 MSI RC 100 kHz – 48 MHz HSI-SYSCLKto I2Cx x=1,2,3 to LPTIMx HSIto SWPMI MSI PCLK2 HSI APB2 PLL / M HSE to APB2 peripherals PRESC / 1,2,4,8,16 PLLSAI3CLK / P PLLUSB1CLK /Q to TIMx PLLCLK /R x=1,8,15,16,17 to
USART1 PLLSAI1 PLLSAI1CLK / P PLLUSB2CLK /Q MSI 48 MHz clock to USB, RNG, SDMMC PLLADC1CLK / R SYSCLK to ADC PLLSAI2 PLLSAI2CLK / P /Q to SAI1 PLLADC2CLK / R SAI1_EXTCLK to SAI2

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SAI2 EXTCLK